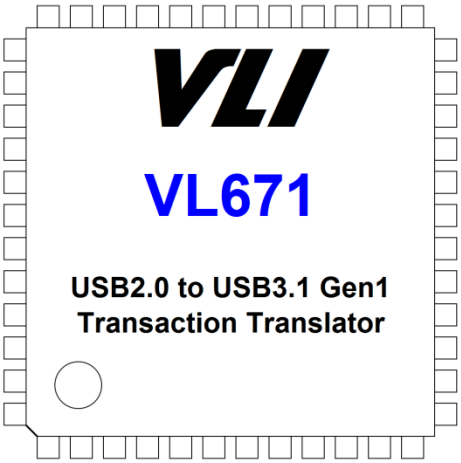
VIA Labs, Inc.

Data Sheet

VL671
Low Power USB 2.0 to USB 3.1 Gen1 Transaction Translator

September 03, 2018

Revision 0.80



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Revision History

Rev	Date	Note	Initial
0.80	09/03/2018	Preliminary release	HC

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Product Features

VL671
Low Power High-Speed USB to Super-Speed USB Transaction Translator

■Super-Speed USB (5Gb/s) and High-Speed USB (480Mb/s)

-Compliant to Universal Serial Bus 3.1 Specification Revision 1.0, Gen1 Mode

-Compliant to Universal Serial Bus Specification Revision 2.0

-Support converting Bulk-Only Transport/Control/Interrupt/Isochronous type transaction between USB 2.0 and USB 3.1 protocol

-Downstream port support USB 2.0 Hub

-Integrated in-house Super-Speed USB PHY and USB 2.0 PHY

■High Performance ARM Cortex-M3 Microprocessor

-Powerful ARM 32-bit energy efficient processor

■Built-in Voltage Regulators

-5.0V to 3.3V LDO

-5.0V to 1.2V switching DC-DC

■GPIOs for Special Function Usage

-8 GPIOs for customer special usage

-UART interface that shared with GPIOs

■Misc

-Support power saving mode

-Support external SPI flash for firmware upgrade

-Integrated PLL with external 25MHz crystal

■Physical

-QFN 48L green package (6x6x0.85 mm)

-QFN 40L green package (5x5x0.85 mm)

■Applications

-Digital Signage System

-Zero-Client

-Industrial printer

-Mass production system for USB products

-HD smart video surveillance system

-High speed data acquisition system

-Virtual Reality HMD (head-mounted display)

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VL671 System Overview

VIA Lab's VL671 is a unique High-speed USB 2.0 to Super-speed USB 3.1 Gen1 transaction translator. VL671 effectively converts USB High-speed transactions to Super-speed transactions and vice-versa. With this capability, VL671 enables USB 2.0 devices to work under a USB 3.1 downstream port which only provides Super-speed interface (no USB 2.0 capability under this USB 3.1 downstream port for specific reasons). Unlike all connected USB 2.0 devices share single 480Mb/s bandwidth on the regular USB 2.0 bus, the VL671-enabled USB 2.0 device have whole 480Mb/s bandwidth for its own use since the upstream of VL671 has converted to the Super-speed USB transaction whose communication protocol is point-to-point based.

To provide best user experience, VL671 also provides bypass mode. When the upstream port of the VL671 is connected to an USB 2.0 downstream port, the USB 2.0 signals are bypassed from the upstream port to the downstream port directly, and vice-versa. In the case that a Super-speed capable device is attached to the downstream port of the VL671, the Super-speed signals are bypassed from the upstream to the downstream port, and vice-versa. (Super-speed bypass mode only available on QFN48) The signal switches to enable the bypass mode are integrated in the VL671.

VL671 integrates in-house Super-speed PHY and USB 2.0 PHY and employs a very powerful ARM-based 32-bit microprocessor which allows the VL671 to quickly convert transactions/protocols between USB 2.0 and USB 3.1 with minimal delay. The external SPI ROM provides the flexibility for future firmware update and customization. GPIO pins and UART interface are supported to satisfy the requirements for different applications. VL671 works perfectly with a single power input from USB 5V bus to save customer BOM cost and is available on QFN 48L (6x6x0.85 mm) and QFN 40L (5x5x0.85 mm) green package.

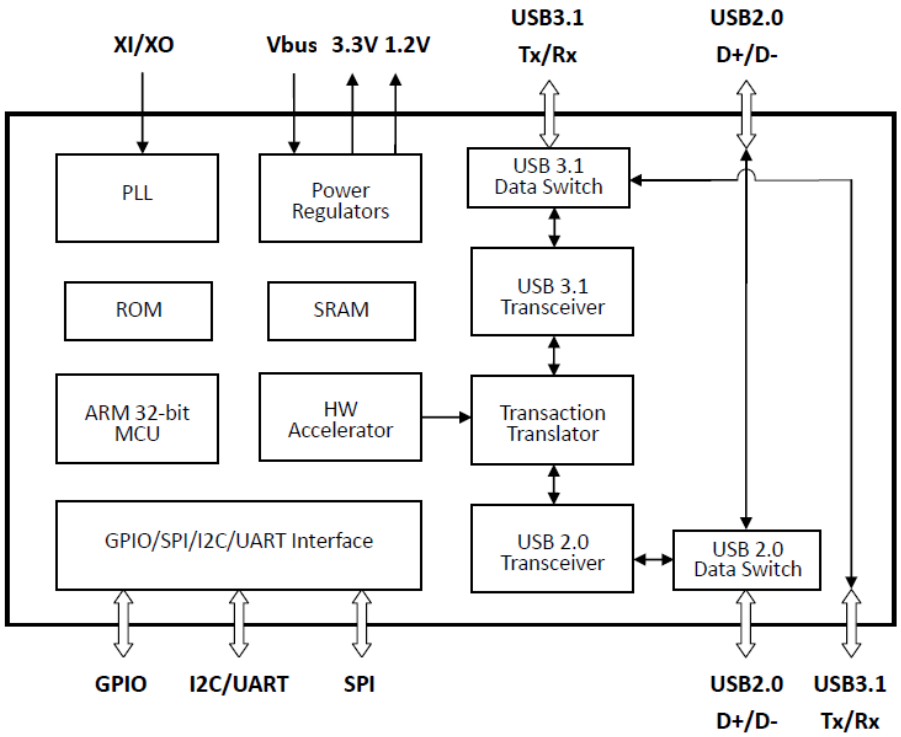

Figure 1 – VL671 Block Diagram

Pinout

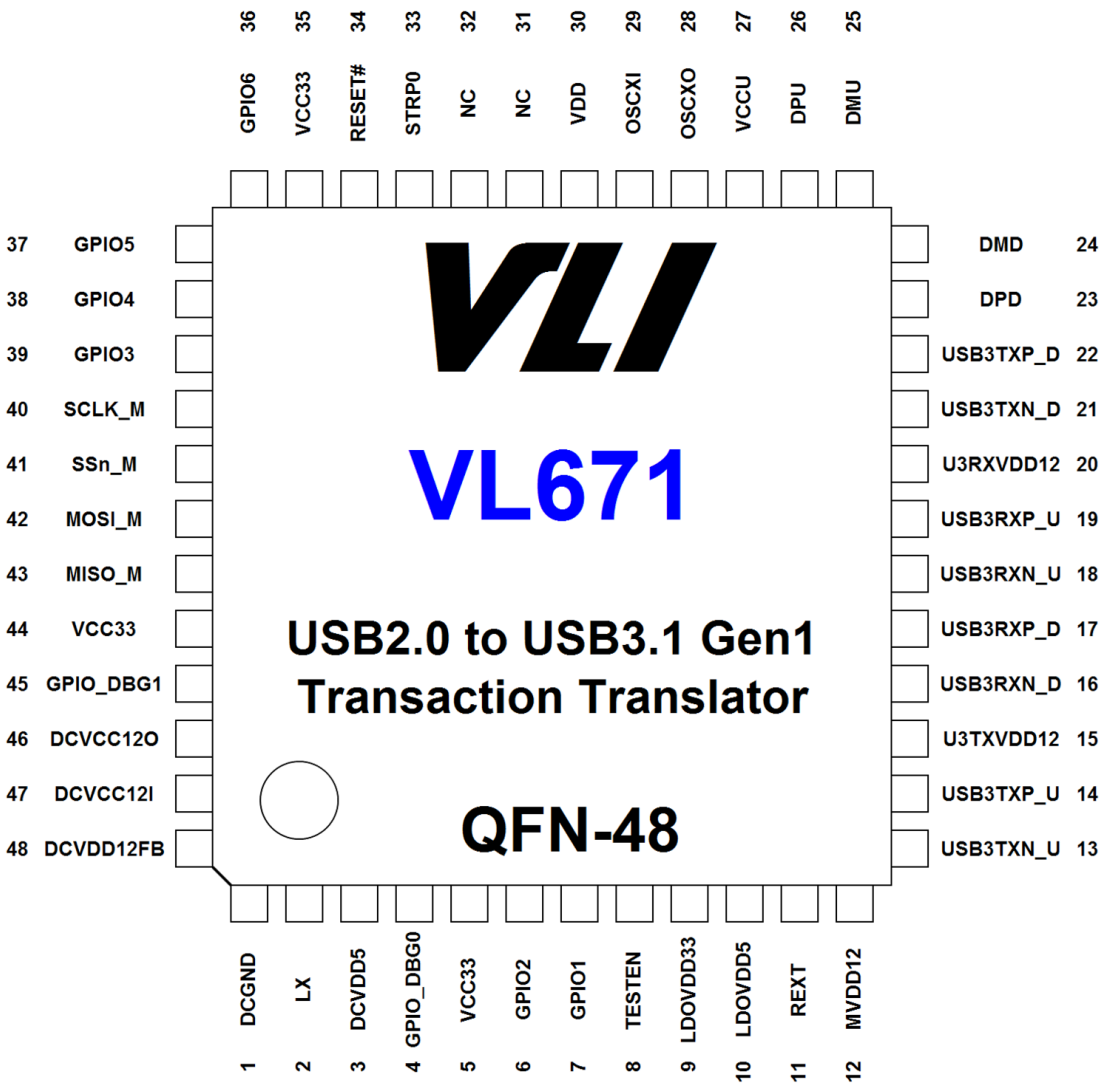

Figure 2 – VL671 QFN-48 Pin Diagram

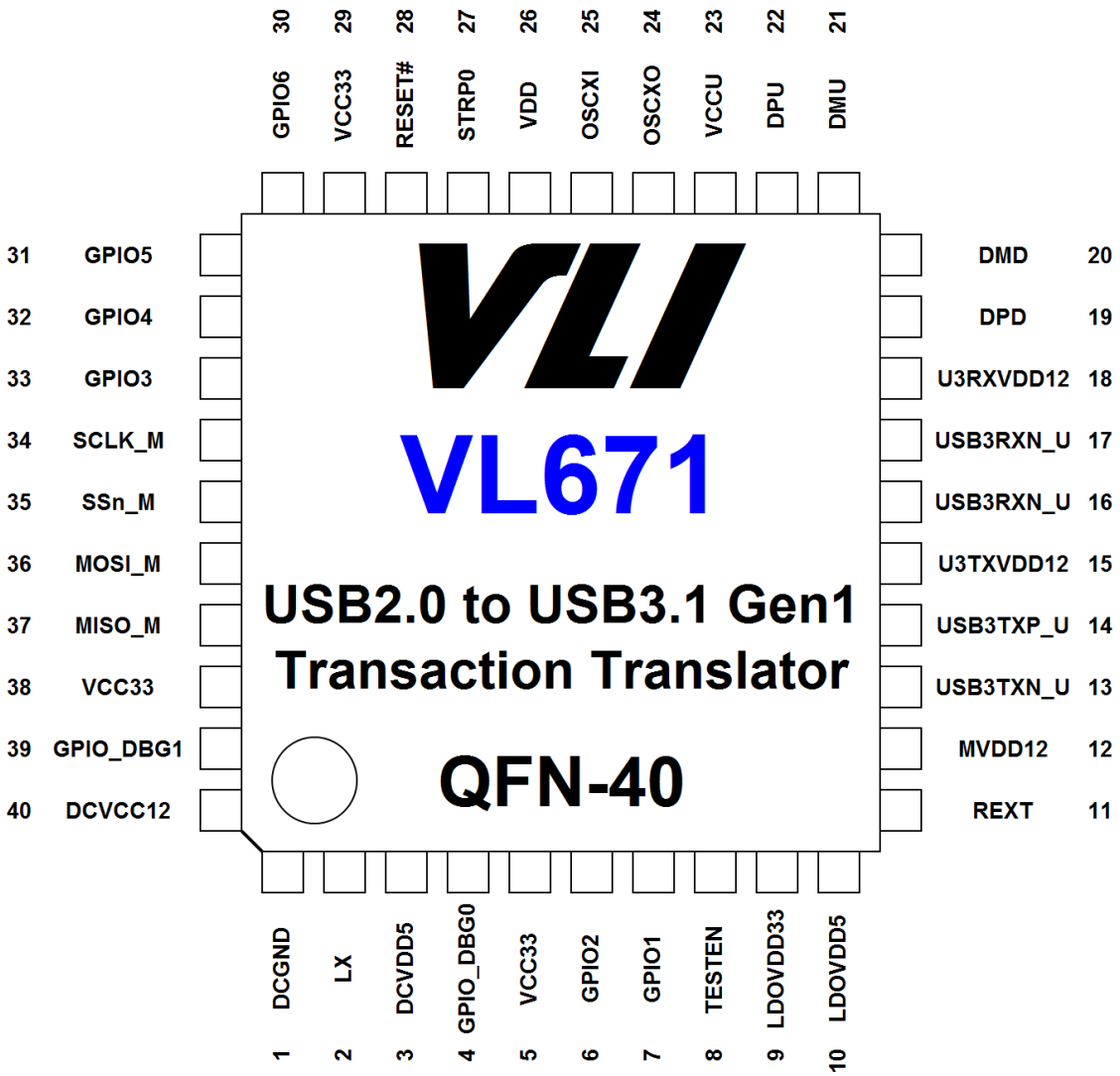

Figure 3 – VL671 QFN-40 Pin Diagram

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Pin List

Table 1 – VL671 QFN-48 Pin List

Pin	Pin Name	Pin	Pin Name
1	DCGND	25	DMU
2	LX	26	DPU
3	DCVDD5	27	VCCU
4	GPIO_DBG0	28	OSCXO
5	VCC33	29	OSCXI
6	GPIO2	30	VDD
7	GPIO1	31	NC
8	TESTEN	32	NC
9	LDOVDD33	33	STRP0
10	LDOVDD5	34	RESET#
11	REXT	35	VCC33
12	MVDD12	36	GPIO6
13	USB3TXN_U	37	GPIO5
14	USB3TXP_U	38	GPIO4
15	U3TXVDD12	39	GPIO3
16	USB3RXN_D	40	SCLK_M
17	USB3RXP_D	41	SSn_M
18	USB3RXN_U	42	MOSI_M
19	USB3RXP_U	43	MISO_M
20	U3RXVDD12	44	VCC33
21	USB3TXN_D	45	GPIO_DBG1
22	USB3TXP_D	46	DCVCC12O
23	DPD	47	DCVCC12I
24	DMD	48	DCVDD12FB

Table 2 – VL671 QFN-40 Pin List

Pin	Pin Name	Pin	Pin Name
1	DCGND	21	DMU
2	LX	22	DPU
3	DCVDD5	23	VCCU
4	GPIO_DBG0	24	OSCXO
5	VCC33	25	OSCXI
6	GPIO2	26	VDD
7	GPIO1	27	STRP0
8	TESTEN	28	RESET#
9	LDOVDD33	29	VCC33
10	LDOVDD5	30	GPIO6
11	REXT	31	GPIO5
12	MVDD12	32	GPIO4
13	USB3TXN_U	33	GPIO3
14	USB3TXP_U	34	SCLK_M
15	U3TXVDD12	35	SSn_M
16	USB3RXN_U	36	MOSI_M
17	USB3RXP_U	37	MISO_M
18	U3RXVDD12	38	VCC33
19	DPD	39	GPIO_DBG1
20	DMD	40	DCVCC12

Pin Descriptions

Signal Type Definition

Name	Type	Signal Description
Input	I	A standard input-only signal
Output	O	A standard active driver
Input/Output	I/O	A bi-directional signal
Analog bias	A_{BIAS}	Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network
Power	PWR	A power pin
Ground	GND	A ground pin

Upstream USB Interface

Pin Name	QFN48	QFN40	I/O	Signal Description
USB3TXN_U	13	13	O	USB 3.1 Differential Transmit Data-
USB3TXP_U	14	14	O	USB 3.1 Differential Transmit Data+
U3TXVDD12	15	15	PWR	Analog 1.2V Power
USB3RXN_U	18	16	I	USB 3.1 Differential Receive Data-
USB3RXP_U	19	17	I	USB 3.1 Differential Receive Data+
U3RXVDD12	20	18	PWR	Analog 1.2V Power
DMU	25	21	I/O	USB 2.0 Bus Data Minus(D-)
DPU	26	22	I/O	USB 2.0 Bus Data Plus(D+)

Downstream USB Interface

Pin Name	QFN48	QFN40	I/O	Signal Description
USB3TXN_D	21	—	O	USB 3.1 Differential Transmit Data-
USB3TXP_D	22	—	O	USB 3.1 Differential Transmit Data+
USB3RXN_D	16	—	I	USB 3.1 Differential Receive Data-
USB3RXP_D	17	—	I	USB 3.1 Differential Receive Data+
DMD	24	20	I/O	USB 2.0 Bus Data Minus(D-)
DPD	23	19	I/O	USB 2.0 Bus Data Plus(D+)
VCCU	27	23	PWR	Analog 3.3V Power

Analog Command Block

Pin Name	QFN48	QFN40	I/O	Signal Description
OSCXO	28	24	O	25M crystal output
OSCXI	29	25	I	25M crystal input
REXT	11	11	A_{BIAS}	USB 3.1 reference resistor

Serial EEPROM Interface

Pin Name	QFN48	QFN40	I/O	Signal Description
SCLK_M	40	34	O	Clock for SPI Master; Serial Flash Clock
SSn_M	41	35	O	Chip select for SPI Master; Serial Flash Chip Enable
MOSI_M	42	36	O	MOSI for SPI Master; Serial Flash Data Input
MISO_M	43	37	I	MISO for SPI Master; Serial Flash Data Output

General Purpose I/O and Miscellaneous

Pin Name	QFN48	QFN40	I/O	Signal Description
RESET#	34	28	I	External Chip Reset
STRP0	33	27	I	Mode setting pin 0
NC	32, 31	—	—	Not Connected
GPIO1	7	7	I/O	General purpose input output pin, including PWM
GPIO2	6	6	I/O	General purpose input output pin, including PWM
GPIO3	39	33	I/O	General purpose input output pin
GPIO4	38	32	I/O	General purpose input output pin
GPIO5	37	31	I/O	General purpose input output pin
GPIO6	36	30	I/O	General purpose input output pin
GPIO_DBG0	4	4	I/O	General purpose input output pin
GPIO_DBG1	45	39	I/O	General purpose input output pin

Test Pin

Pin Name	QFN48	QFN40	I/O	Signal Description
TESTEN	8	8	I	Test Mode Enable

Power and Ground

Pin Name	QFN48	QFN40	I/O	Signal Description
DCGND	1	1	GND	Ground for internal DC-DC regulator
LX	2	2	O	1.2V voltage output for internal DC-DC regulator
DCVDD5	3	3	PWR	5.0V voltage input for internal DC-DC regulator
VCC33	5,35,44	5,29,38	PWR	3.3V IO power
LDOVDD33	9	9	PWR	3.3V voltage output for 5V to 3.3V LDO
LDOVDD5	10	10	PWR	5.0V voltage input for 5V to 3.3V LDO
MVDD12	12	12	PWR	1.2V Master analog power
VDD	30	26	PWR	1.2V Core power
DCVCC12O	46	—	PWR	1.2V voltage for core power
DCVCC12I	47	—	PWR	1.2V voltage for core power
DCVDD12FB	48	—	I	1.2V feedback for internal DC-DC regulator
DCVCC12	—	40	PWR	1.2V voltage for core power

Electrical Specification

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-55	125	°C	—
T_A	Ambient Temperature	0	70	°C	—
DCVDD5	Power Supply Voltage of 5V to 1.2V DC-DC	-0.3	5.5	V	—
LDOVDD5	Power Supply Voltage of 5V to 3.3V LDO	-0.3	5.5	V	—
V_{IN}	Input Voltage at I/O pins	-0.3	3.63	V	—
V_{ESD}	Electrostatic Discharge	—	2	kV	Human Body Model

Note: Stress above conditions may cause permanent damage to the device.

Functional operation of this device should be restricted to the conditions described.

Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
DCVDD5	Power Supply Voltage of 5V to 1.2V DC-DC	4.5	5	5.5	V
LDOVDD5	Power Supply Voltage of 5V to 3.3V LDO	4.5	5	5.5	V
V_{CC33}	Digital IO power 3.3V	3.135	3.3	3.465	V
V_{CC12}	Digital Core power 1.2V	1.14	1.2	1.26	V
DCGND	Ground	—	0	—	V

General IO DC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.30	0.8	V	—
V_{IH}	Input High Voltage	2.0	3.6	V	—
V_{OL}	Output Low Voltage	—	0.4	V	IOL=15.8mA
V_{OH}	Output High Voltage	2.4	—	V	IOH=26.5mA

Internal 5V to 1.2V DC/DC Converter

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	4.5	5.0	5.5	V	
Output Voltage	1.14	1.2	1.26	V	
Max. Output Current		450	520	mA	
Output Voltage Tolerance		+/- 5%			

Internal 5V to 3.3V LDO Regulator

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	4.5	5.0	5.5	V	
Output Voltage	3.135	3.3	3.465	V	
Max. Output Current		50	100	mA	
Output Voltage Tolerance		+/- 5%			

External Crystal Electrical Characteristics

Please refer to the Figure 4.

Symbol	Parameter	Min	Typ	Max	Unit
FL	Normal Frequency		25		MHz
	Oscillation Mode		Fundamental		
	Frequency Tolerance	-30		30	ppm
	Aging	-5		5	ppm
CL	Loading Capacitance		12		pf
C0	Shunt Capacitance	1	3	7	pf
Rr	Effective Resistance			50	ohms

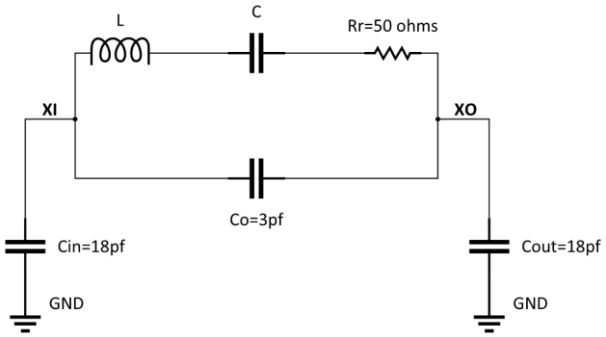
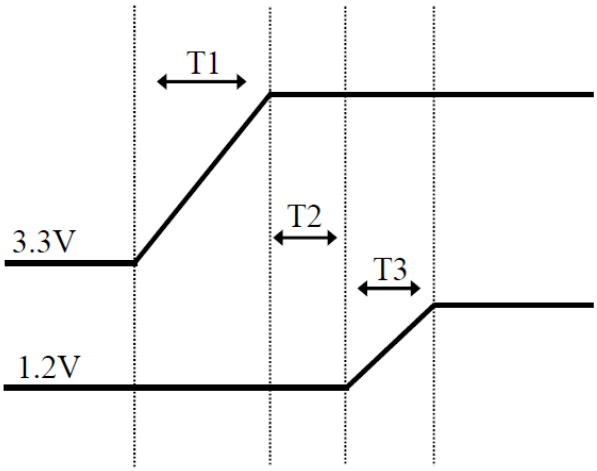


Figure 4 – 25MHz Crystal equivalent circuit and spec requirement

VL671 Built-in Regulator Power Sequence



Time	Min	Max
T1	~	14ms
T2	0	2ms
T3	~	1.6ms

Note: Based on Vbus rising time = 20ms

VL671 power sequence is Vbus -> 3.3V -> 1.2V.
Built-in 3.3V regulator is activated when Vbus is reaching 0.8V.

T1: 3.3V Rising time (0%-100%)
T2: Time interval between 3.3V and 1.2V
T3: 1.2V Rising time (0%-100%)

USB Full Speed DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{FSIH}	Full-speed Input High	2.0		V	—
V_{FSIL}	Full-speed Input Low		0.8	V	—
V_{FSCM}	Differential Common Mode Voltage	0.8	2.5	V	—
V_{FSOL}	Full-speed Output Low	0.0	0.3	V	—
V_{FSOH}	Full-speed Output High	2.8	3.6	V	—
T_{FSR}	Full-speed Rise Time	4	20	ns	—
T_{FSF}	Full-speed Fall Time	4	20	ns	—
V_{FSCRS}	Full-speed Output Signal Crossover Voltage	1.3	2.0	V	—

USB High Speed DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{HSSQ}	High-speed squelch detection threshold	100	150	mV	—
V_{HSCM}	High-speed data signaling common mode voltage	-50	500	mV	—
V_{HSOI}	High-speed idle level	-10	10	mV	—
V_{HSOH}	High-speed data high	360	440	mV	—
V_{HSOL}	High-speed data low	-10	10	mV	—
V_{CHIRPJ}	Chirp J level	700	1100	mV	—
V_{CHIRPK}	Chirp K level	-900	-500	mV	—
Z_{HSDRV}	Drive output resistance	40.5	49.5	Ω	—
T_{HSR}	High-speed Rise Time	500		ps	—
T_{HSF}	High-speed Fall Time	500		ps	—

USB Super Speed TX Characteristics

Symbol	Parameter	Min	Max	Unit	Note
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p Tx swing	0.8	1.2	V	—
$V_{TX\text{-}DE\text{-}RATIO}$	Tx de-emphasis	3.0	4.0	dB	—
$R_{TX\text{-}DIFF\text{-}DC}$	DC differential impedance	72	120	Ω	—
$V_{TX\text{-}RCV\text{-}DETECT}$	The Voltage Change allowed during Receiver Detection		0.6	V	—
$T_{TX\text{-}EYE}$	Transmitter Eye	0.625		UI	—
$T_{TX\text{-}DJ\text{-}DD}$	Tx Deterministic Jitter		0.205	UI	—
$R_{TX\text{-}DC}$	Transmitter DC Common Mode Impedance	18	30	Ω	—
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0	2.2	V	—
$V_{TX\text{-}CM\text{-}AC\text{-}PP\text{-}ACTIVE}$	Tx AC Common Mode Voltage Active		100	mV	—
$V_{TX\text{-}IDLE\text{-}DIFF\text{-}AC\text{-}pp}$	Electrical Idle Differential P-P Output Voltage	0	10	mV	—
$V_{TX\text{-}IDLE\text{-}DIFF\text{-}DC}$	DC Electrical Idle Differential Output Voltage	0	10	mV	—

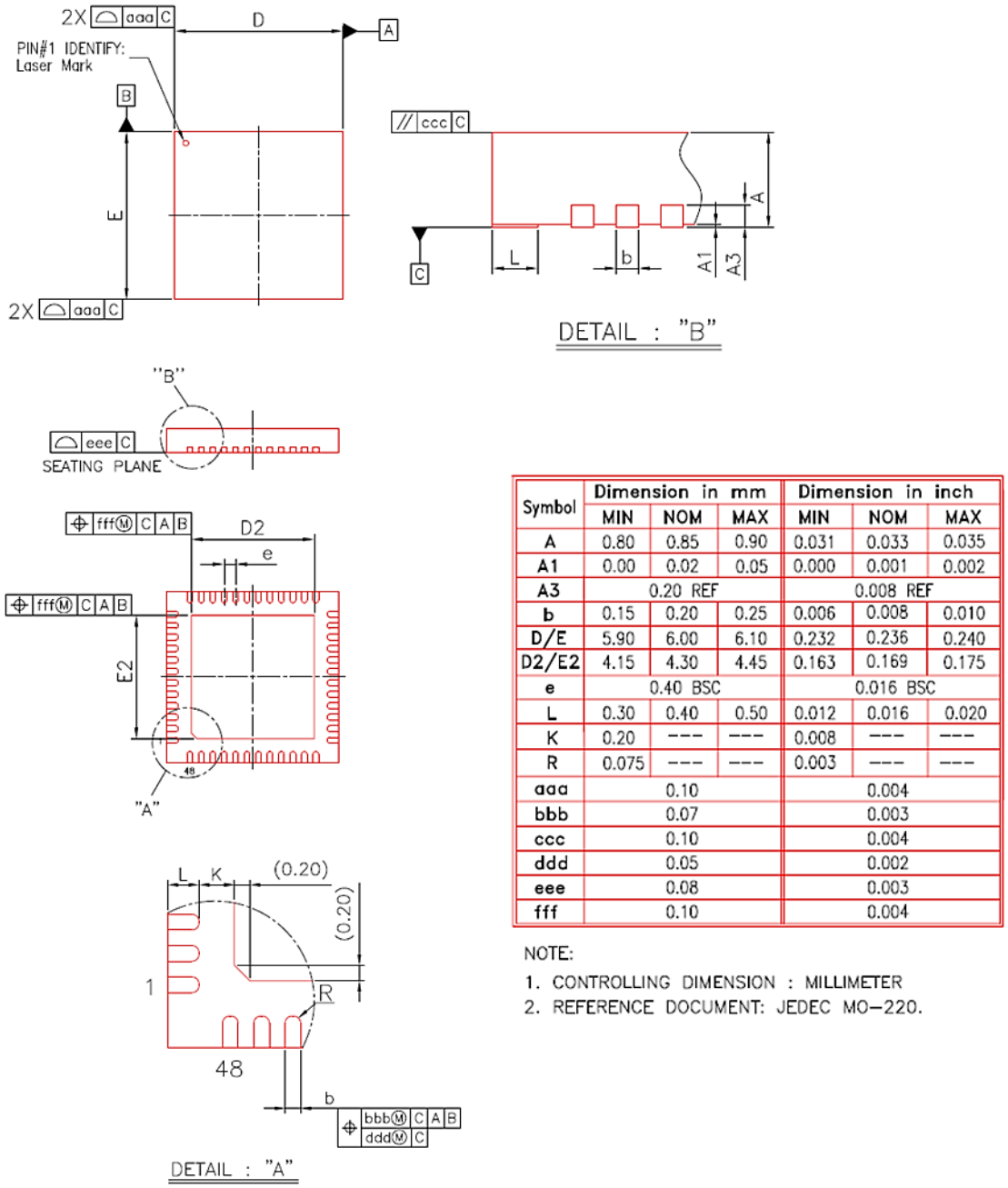
USB Super Speed RX Characteristics (5.0 GT/s)

Symbol	Parameter	Min	Max	Unit	Note
UI	Unit Interval	199.94	200.06	ps	UI does not account for SSC caused variations
R_{RX-DC}	Receiver DC common mode impedance	18	30	Ω	DC impedance limits are needed to guarantee Receiver detect Measured with respect to ground over a voltage of 500mV maximum
$R_{RX-DIFF-DC}$	DC differential impedance	72	120	Ω	
$Z_{RX-HIGH-IMP-DC-POS}$	DC Input CM Input Impedance for V>0 during Reset or power down	25k		Ω	Rx DC CM impedance with the Rx terminations not powered, measured over the range 0 – 500mv with respect to ground
$V_{RX-LFPS-DET-DIFF_{p-p}}$	LFPS Detect Threshold	100	300	mV	Below the minimum is noise Must wake up above the maximum
$V_{RX-DIFF-PP-POST-EQ}$	Differential Rx peak-to-peak voltage	30		mV	Measured after the Rx EQ function (Section 6.8.2)
t_{RX-TJ}	Max Rx inherent timing error		0.45	UI	Measured after the Rx EQ function (Section 6.8.2)
$t_{RX-DJ-DD}$	Max Rx inherent deterministic timing error		0.3	UI	Maximum Rx inherent deterministic timing error
$C_{RX-PARASITIC}$	Rx input capacitance for return loss		1.1	pf	
$V_{RX-CM-AC-P}$	Rx AC common mode voltage		150	mV Peak	Measured at Rx pins into a pair of 50Ω terminations into ground Includes Tx and channel conversion, AC range up to 5 GHz
$V_{RX-CM-DC-ACTIVE-IDLE-DELTA-P}$	Rx AC common mode voltage during the U1 to U0 transition		200	mV Peak	Measured at Rx pins into a pair of 50Ω terminations into ground Includes Tx and channel conversion, AC range up to 5 GHz

Package Mechanical Specifications

QFN-48 Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	250	°C
Max Time within 5°C of Tp	30	seconds



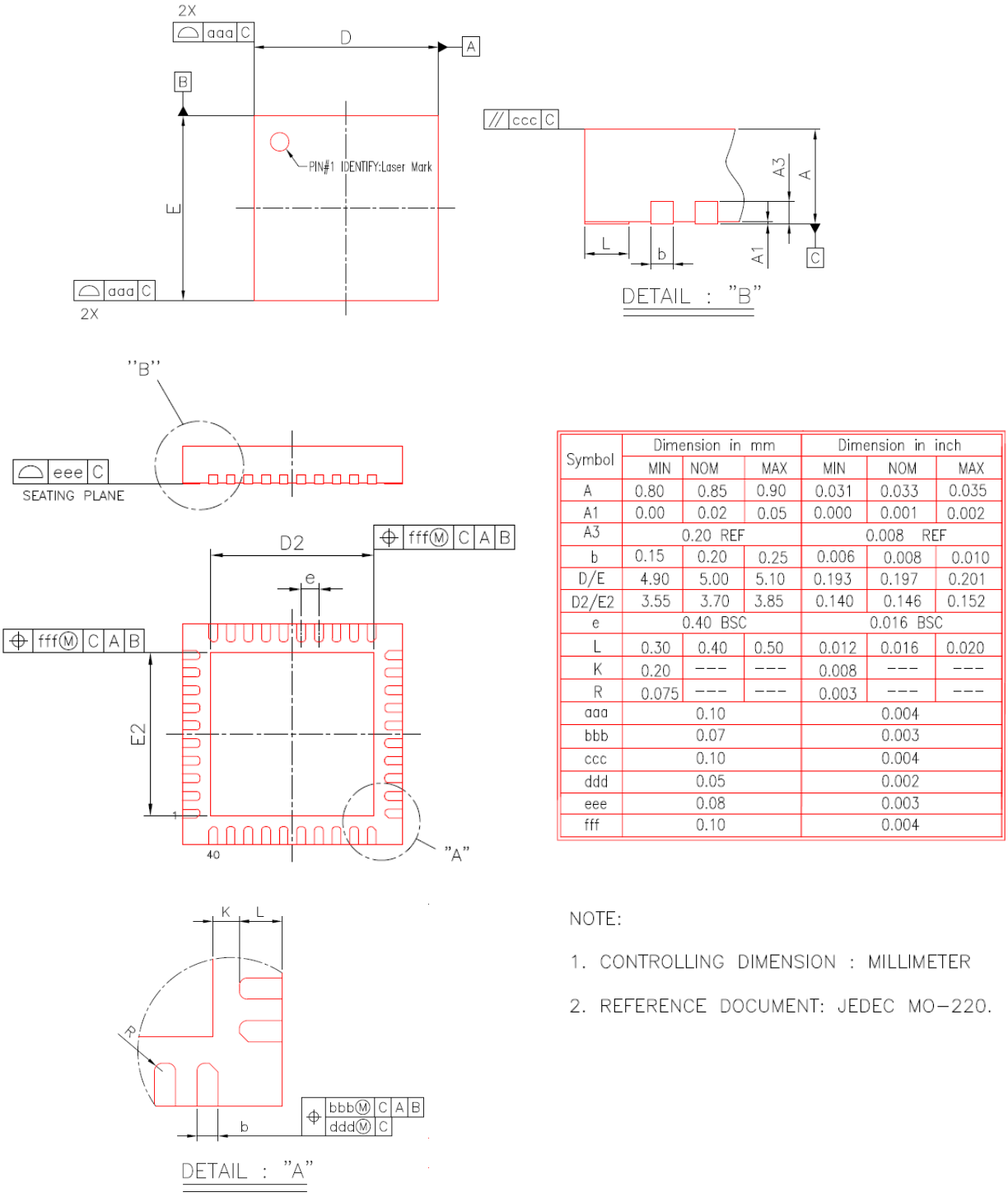
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
D2/E2	4.15	4.30	4.45	0.163	0.169	0.175
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa		0.10			0.004	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	
fff		0.10			0.004	

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 5 – QFN 48L 6x6x0.85 mm Mechanical Specification

QFN-40 Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	250	°C
Max Time within 5°C of Tp	30	seconds



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	4.90	5.00	5.10	0.193	0.197	0.201
D2/E2	3.55	3.70	3.85	0.140	0.146	0.152
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa		0.10			0.004	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	
fff		0.10			0.004	

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 6 – QFN 40L 5x5x0.85 mm Mechanical Specification

Package Top Side Marking

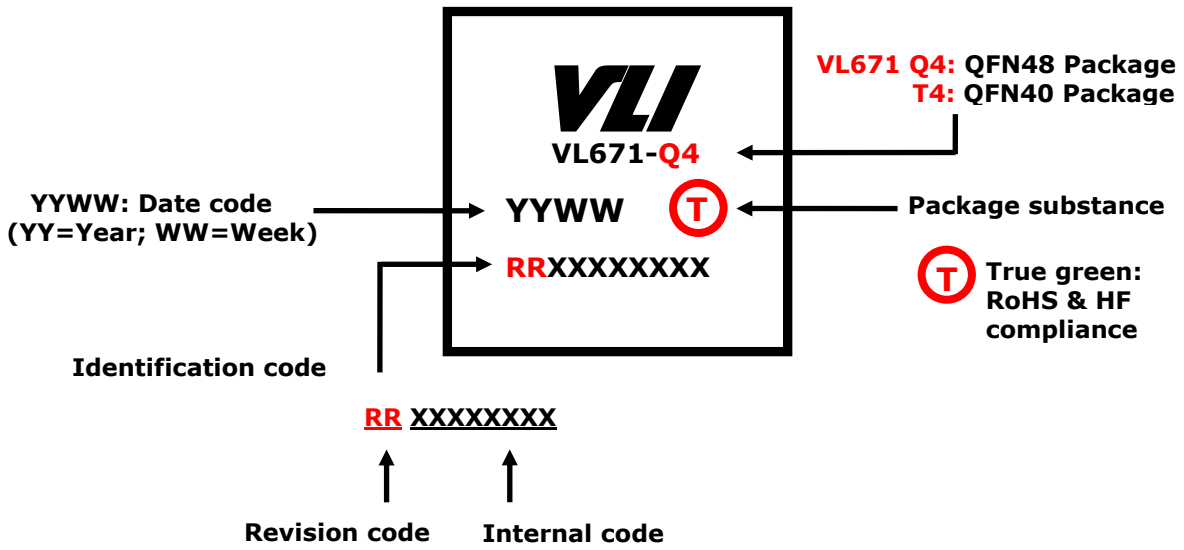


Figure 7 – VL671 Package Top Side Marking

Ordering Information

Please contact VIA Labs sales representative or distributor in your region for ordering part number details.